

# High Yield X-Band GaAs Power MMIC Insertion into the 160-W MODAR Wind Shear Detection/Weather System

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**Abstract**—This paper describes the successful insertion of a high yield 4-W GaAs X-band power MMIC into the solid-state transmitter of the MODular Avionics Radar (MODAR) weather system. To date, over 15 000 4-W MMIC's have been delivered with a combined dc/RF test yield averaging 39%. The design and fabrication of the MMIC's are presented along with statistical test data on over 46 000 MMIC's. The integration of the MMIC's into a higher level 12-W hybrid assembly and an 85-W power module are also discussed. Two 85-W modules are combined in the transmitter to achieve a nominal power output of 160 W. Statistical test data on these higher level assemblies is presented. This work demonstrates the viability of inserting GaAs power MMIC's into commercial systems.

## I. INTRODUCTION

THE advantages of using solid-state power amplifiers for airborne applications are well known. Power amplifier modules using GaAs MMIC's, for example, are smaller in size, lighter in weight and lower in phase noise than a comparable TWT amplifier. MESFET-based MMIC's also have a well demonstrated reliability record [1]. However, to achieve commercial viability, a solid-state amplifier must not only exhibit good RF performance but be low cost as well. For MMIC insertion this requirement translates to robust design and high processing yields.

This paper describes the design, fabrication and insertion of a high yield, 4-W X-band GaAs MMIC into the 160-W solid-state transmitter of the MODAR airborne weather system. MODAR offered an ideal opportunity for the insertion of GaAs MMIC technology into a commercial product. The system and the higher level power amplifier assemblies were designed so that state-of-the-art performance was not required from the MMIC's. The challenges for the MMIC design and fabrication, therefore, were to take advantage of this situation in order to maximize overall yield including line yield, dc yield, RF yield and QC (quality control) yield. Section II of the paper contains a brief description of the MODAR system capabilities and requirements. Section III discusses the design, fabrication and

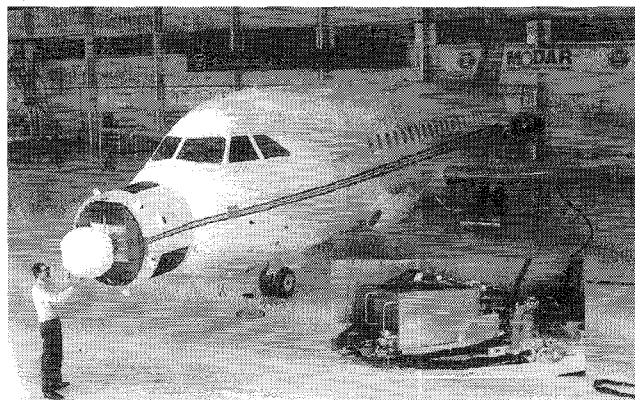


Fig. 1. Photo of the MODAR weather radar installed on a BAC 1-11 test aircraft.

test of the 4-W power MMIC with the major emphasis on those issues which affected the MMIC dc and RF yields. Statistical data demonstrating the high yield design/fabrication approach is presented on over 46 000 MMIC's tested to date. Sections IV and V briefly discuss the integration of these MMIC's into the higher level assemblies which comprise the MODAR solid-state transmitter. These sections should provide better insight into the place of the power MMIC in the overall system and an appreciation for the concurrent engineering efforts required in a commercial environment.

## II. THE MODAR WEATHER SYSTEM

In 1991, Westinghouse embarked on a new product line aimed at both the military and commercial markets. The need for this system, MODAR (MODular Avionics Radar), came from a commercial aviation hazard called wind shear which has been known to cause many disasters with loss of life. Prior to this time, existing technology could only warn that the aircraft was in a wind shear event. The MODAR system added the predictability that an event would happen.

A family of wind shear detection radar systems was developed out of the design efforts (Fig. 1). The MODAR-3000 was intended for the commercial market, while the MODAR-4000 was directed at the military tanker/transport market. Additional features in the MODAR-3000 system include ARINC-708 weather radar functions and basic ground map. The MODAR-4000 includes these functions in addition to high resolution

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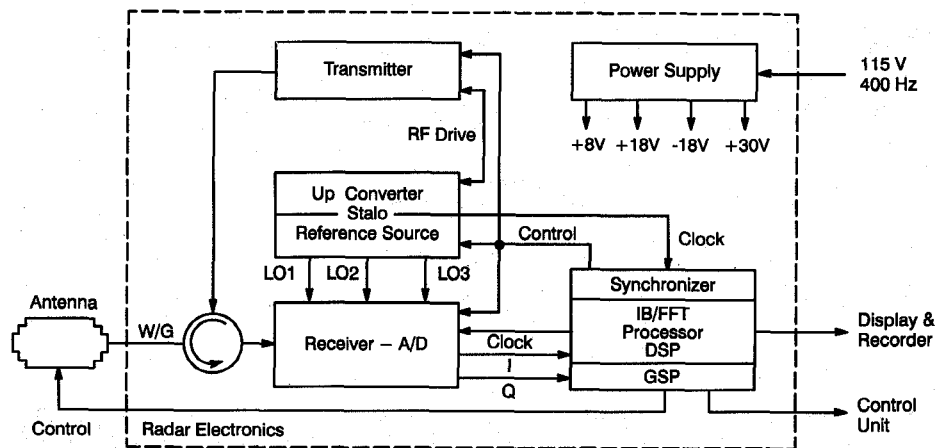


Fig. 2. Block diagram of the MODAR modular radar architecture.

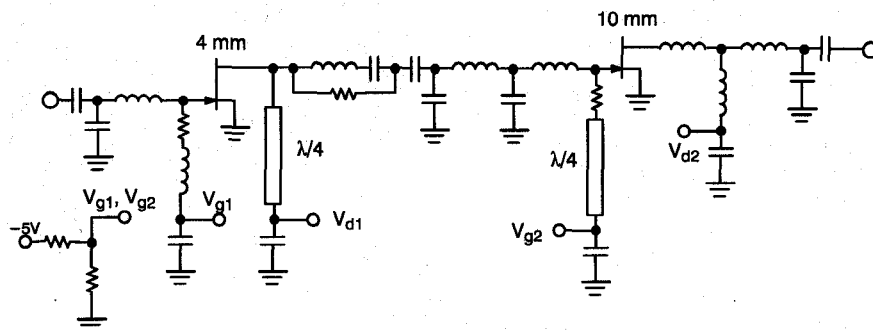


Fig. 3. Schematic diagram of the two-stage 4-W X-band power MMIC. The design employs a 4-mm input stage FET and a 10-mm output stage FET.

ground map with precision update capability, airborne target detection and beacon detection. All of the systems include a highly reliable 160-W solid-state transmitter (Fig. 2).

At the heart of the 160-W transmitter is a pair of 85-W solid-state X-band power modules covering the 9.3 to 9.41-GHz band. Each 85-W module consists of 11-hybrid power amplifier assemblies with a nominal power output of 12 W. The 12-W power amplifiers are fabricated by combining four 4-W X-band GaAs MMIC's designed specially for this application. Each transmitter, therefore, employs 88 4-W MMIC's. Specifications for the power MMIC's were based on the described power combining architecture and the system radar modes. These specifications include minimum power output during the long pulse radar mode, maximum drain current during the short pulse radar mode, maximum gate current, compression characteristics and associated gain. As mentioned, a key factor in making this system commercially viable was a transmitter architecture which kept the MMIC specifications well within reach of current technology.

### III. 4 W X-BAND POWER MMIC

#### A. 4-W MMIC Design

Performance requirements for the MODAR system filtered down from the 85-W modules to a 4-W MMIC building block covering the 9.3 to 9.41-GHz band. Initial specs were set to begin the design. Later, as MMIC's were fabricated and inserted into the 12-W hybrid amplifiers, it was discovered

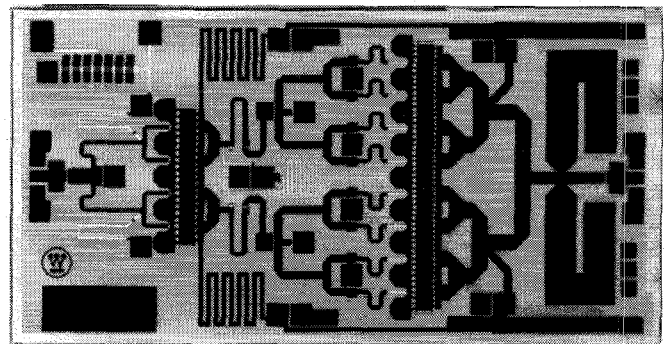


Fig. 4. Photo of the 4-W X-band power MMIC. Chip size is .163" x .084".

that some specs could be relaxed in order to further improve RF yield.

A schematic diagram of the 4-W MMIC building block is shown in Fig. 3. The basic chip design philosophy took full advantage of the fairly liberal MMIC specification window in order to maximize RF yield. The two-stage chip employs a 4-mm input stage FET and a 10-mm output stage FET. This 2.5:1-ratio of output to input device periphery, though conservative, ensures that an adequate output FET drive power margin will be available to compensate for lot-to-lot wafer processing variations. As shown in Fig. 4, all matching circuitry (input, interstage, output) is included on-chip. This allows complete RF testing and yielding to customer specifications to be performed on-wafer.

The output 10-mm FET is a continuous structure with eight input and output feed points. In a similar fashion, the 4-mm input device is a continuous structure with four input/output feeds. This approach results in a more compact device and eliminates the possibility of odd mode oscillations [2]. An in-house thermal modeling program [3] was used to calculate maximum junction temperatures and set the device gate pitches. The input FET gate pitch was set at 22- $\mu\text{m}$  and the output FET gate pitch was set at 18- $\mu\text{m}$ . For the 18- $\mu\text{m}$  gate pitch FET, the calculated junction temperature rise was 61°C under CW (or long pulse) conditions. The eight output feed points are combined using a corporate combiner output matching network. To reduce processing sensitivity, improve yield and reduce output circuit losses, a large open-circuited stub is used in the output network instead of a shunt MIM capacitor to ground. From an overall yield viewpoint, the improved RF performance gained by using the stub justified the resultant increase in chip size. In order to minimize the number of design iterations, the stub arrangement, as well as most of the other matching circuitry on the chip, was analyzed using the electromagnetic simulator software EM (Sonnet software).

The bandwidth of the critical interstage matching network was widened to 1.5 GHz to reduce the sensitivity of the output FET drive to MIM capacitance and  $C_{gs}$  variations. The completed interstage circuit is essentially two identical circuits in parallel. Each half transforms the input impedance of a 5-mm FET (half of the 10-mm output device) up to the optimum power match impedance of a 2-mm FET (half of the 4-mm input device). A simple single-tuned L-C network is used for input tuning. Future modifications to the chip design could include a less sensitive double-tuned input network.

A resistive voltage divider is included on each chip to drop the -5-V module gate supply to the  $\approx -1.6$ -V gate voltage required by each MMIC. Chip bias is set for class AB operation to improve efficiency [4]. This reduced the complexity of the bias arrangement at the 12-W amplifier level and provided flexibility in biasing the four MMIC's which comprise each 12-W amplifier. Initially, in anticipation of possible process drift, the voltage divider was made adjustable with seven taps at 0.2-V increments so that optimum bias could be set for each MMIC. The optimum bias was determined from on-wafer dc probing. Evaluation of data from the first MMIC fabrication runs demonstrated, however, that the FET gate voltage was uniform enough from lot to lot that the fixed -1.6-V setting could be used. This further reduced test and assembly costs. Bond pads for both RF and dc connections were sized for automated assembly of the 12-W amplifiers. A ground-signal-ground RF probe pad at the input and output of the MMIC is used for on-wafer power testing. As mentioned, each chip is fully tested on-wafer for spec compliance. The size of the MMIC is .163"  $\times$  .084"  $\times$  .004".

A plot of power output and power-added efficiency (PAE) vs. frequency for the 4-W chip is shown in Fig. 5. For this measurement, the chip was operated at 9-V pulsed drain bias with a 20- $\mu\text{sec}$  pulse width and a 25% duty cycle. A power output of over 36-dBm (4 W) with greater than 30% PAE is typical over the 9.3–9.41-GHz band.

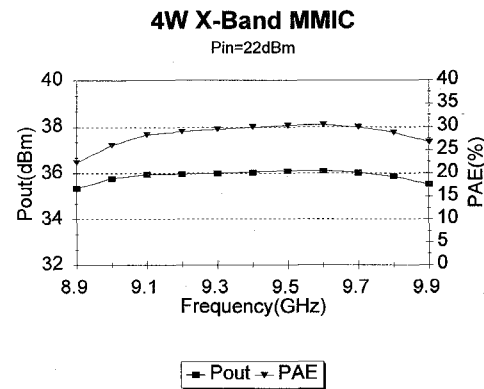


Fig. 5. Power output and power-added efficiency plots versus frequency for a typical 4-W MMIC. The drain was pulsed at 9 V with a 20  $\mu\text{sec}$  pulse width and a 25% duty cycle.

### B. Process and FET Description

The MODAR X-band power MMIC was designed based on a baseline X-band power MESFET process which has been used for other previously described X-band power applications [5], [6]. The active element is a power MESFET fabricated using conventional GaAs processing techniques including oxygen damage implants for isolation, AuGe/Ni/Au alloyed ohmic contacts, a double ledge process to increase drain-gate breakdown voltage, direct-written 0.5- $\mu\text{m}$  TiPtAu gates, ECR-deposited  $\text{Si}_3\text{N}_4$  passivation, wax mounting onto sapphire discs for lapping to 4 mil final thickness, and reactively ion etched vias. The MESFETs employ a buried spike-doped Lo-Hi profile similar to [7] which is grown using MBE for active-layer uniformity to maximize yield. Typical MESFET performance at 10-GHz, obtained from a mechanical load-pull system and without any specific harmonic tuning, is 450–500 mW/mm saturated power out with >45% power-added efficiency for 9-V drain operation. Passive components included MIM capacitors where the  $\text{Si}_3\text{N}_4$  passivation was also used as the capacitor dielectric, TiPt thin film resistors, ohmic metal resistors, and microstrip transmission lines for distributed circuit elements. This power MESFET process has been through process demonstrations funded by MIMIC Phase 2 which have shaken-out problems, improved throughput, and generally made the process production-ready [8]–[10].

### C. On-Wafer Testing and Statistical Data

A major factor in keeping overall system costs to a minimum is to ensure that all MMIC's used in higher level assemblies are fully spec compliant. Therefore, it is necessary to test the MMIC chips before sending them on to the amplifier assembly operation. This test is most easily performed at the wafer level [11]. Ultimately, this test should be a quick screen of the devices to identify good from bad. However, initially there is no measured data on the performance of the devices to determine which parameter(s) to use for the screen. Therefore, for the first few production buys, full testing of the MMIC's at wafer level is needed.

The MODAR specifications defined the RF power out, a pseudo-compression parameter called saturation, the droop

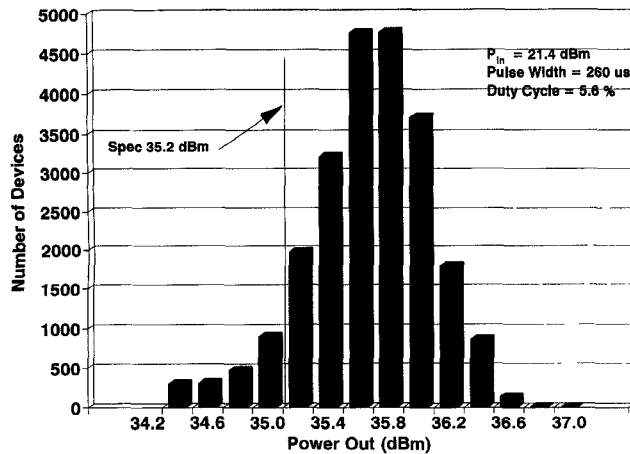


Fig. 6. Power output distribution for 46 000 4-W MMIC's. The mean power output under the worst case longest pulse mode is 35.66 dBm (3.7 W) with a sigma of .41 dB.

of the RF pulse, the gate current and the drain current. The MODAR radar operates in several modes each with different pulse widths and duty cycles. Thus, the wafer test was complicated by the need to test the RF power out using the longest pulse and the drain current using the shortest pulse. These represent the worst case for these parameters. To keep the test time as short as possible, only the parameters necessary to verify compliance with the specification were measured. The measured data was collected automatically and uploaded to a data base for storage. The information is available to the design engineers as well as the process engineers for future reference. It will also be used to determine screening parameters to replace the full RF wafer test in the future.

The test program first checks the gate voltage and current of each MMIC. If either parameter is "out of spec," the program fails the device and moves on to the next site. Next, the RF off drain current is measured. Again, if this parameter is "out of spec," the device is failed and the program moves to the next device. Only if these parameters pass test are the RF characteristics of the device tested. Overall test time for each wafer is thereby kept to a minimum. As mentioned, the automated test program keeps track of which devices pass or fail test. In addition, a fault flag is generated which is stored with the test data in the data base. The fault flag is a binary number in which the reason for failure is encoded. At the end of the test, the program prints out a summary sheet on the quantity of failures and a pass/fail wafer map. In addition, a list of the row/column numbers of the passing devices is also printed to be forwarded to the dicing and selection operation.

To date, over 15 000 MMIC's have been delivered from over 46 000 tested MMIC's. The combined dc/RF test yield, the percentage of the tested die which passed both dc and RF specifications, was 39%. In the beginning of the program when few devices were tested, the random distribution in the measured parameters was not obvious and decisions on yield, performance and cost were being made which were erroneous. A large number of devices are required before the distribution of the performance is identified. Fig. 6 shows the power output

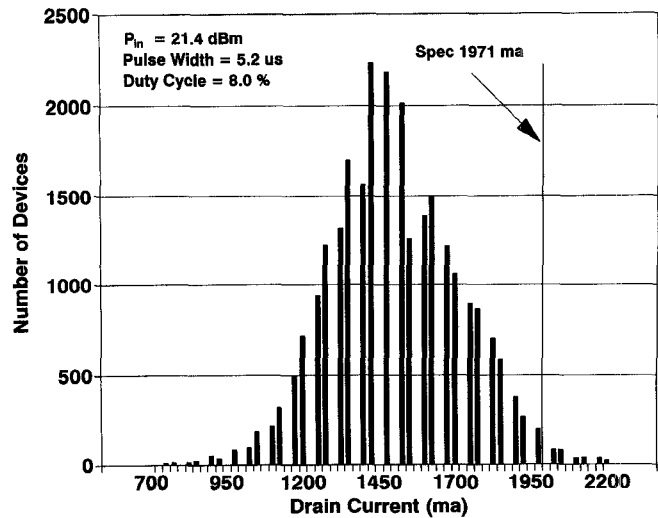


Fig. 7. Drain current distribution for 46 000 4-W MMIC's. The mean current under the worst case shortest pulse mode is 1.49 A with a sigma of .21 A.

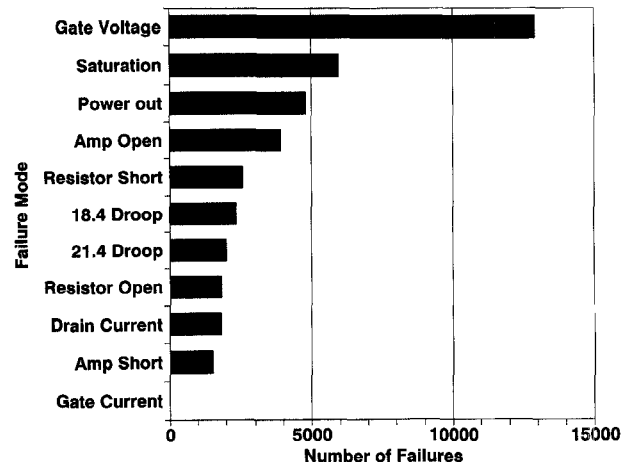


Fig. 8. Pareto chart showing the 4-W MMIC failure mode distribution.

distribution for all of the RF tested MMIC's. As mentioned, this data was taken using the longest pulse width required by the system and represents the worst case (i.e., lowest) power performance. Mean power output is 35.66 dBm ( $\approx 3.7$  W) with a sigma of .41-dB. Also shown on the plot is the lower spec limit of 35.2-dBm. Over 87% of the distribution is above the spec limit. The corresponding drain current distribution is plotted in Fig. 7. Again, this data was taken using the shortest pulse width required by the system and represents the worst case (i.e., highest) MMIC current demand. The low junction temperature of the FETs during the short pulse causes the devices to pull their maximum current. The unequal groupings of current shown in Fig. 7 is due to the non-uniform quantizing of the current measurement during test. The mean current required by the MMIC's is 1.489 A with a sigma of .212 A. The upper spec limit of 1.971 A shown in the figure clearly indicates that high drain current was not a significant yield limiter. In fact, 99% of the devices tested passed the current spec. The result justified the design decision to oversize the input stage FET periphery.

TABLE I  
4-W MMIC PASS/FAIL CRITERIA

Measured Parameter	Pass Condition
Gate Voltage	-1.0 to -3.0 volts
Saturation	$\leq 2.5$ dB
Power Output (long pulse mode)	$\geq 35.2$ dBm
Amplifier (Drain) Open	$I_{\text{drain}} > 1$ mA
Resistor (Voltage Divider) Short	$I_{\text{gate}} \leq 8$ mA
Pulse Droop (18.4 dBm input)	$\leq 1.00$ dB
Pulse Droop (21.4 dBm input)	$\leq 0.75$ dB
Resistor (Voltage Divider) Open	$I_{\text{gate}} > 1$ mA
Drain Current (short pulse mode)	$\leq 1971$ mA
Amplifier (Drain) Short	$I_{\text{drain}} \leq 3$ A
Gate Current	$\leq 8$ mA

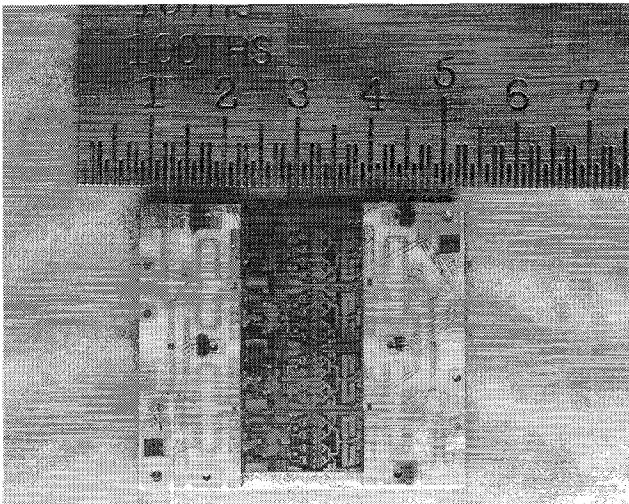


Fig. 9. Photo of the 12-W hybrid power amplifier.

The test fault flag is used to identify the largest yield detractors. Fig. 8 shows a Pareto chart of the MMIC failure modes based on the pass/fail criteria shown in Table I. A device failed if any parameter fell out of the range specified.

Pareto analysis of data accumulated from post-process testing and inspection has been used to guide process improvement efforts. As shown in Fig. 8, the failure category "gate voltage fail" was identified as the major cause of chip loss. This was correlated with current leakage in the gate bias circuit. Failure analysis involving systematic isolation of circuit components identified capacitor leakage as the proximate cause. Based on this, a thorough investigation of the capacitor process was undertaken. This study is continuing; however, an immediate result was the discovery that several process steps were particle generators and that these were compromising capacitor dielectric integrity. These have been corrected and improved capacitor results are anticipated.

#### IV. 12-W POWER AMPLIFIER

The 12-W power amplifier is the first higher level assembly in the MODAR transmitter. As the transmitter architecture was being developed, the quasi-hybrid approach, in which

four fully-matched 4-W MMIC's are combined using thin film networks, was deemed to be the most cost effective way of achieving the intermediate power levels required. Here, concurrent engineering efforts were essential in minimizing assembly costs.

A photo of the 12-W power amplifier is shown in Fig. 9. A balanced amplifier configuration is employed with a divider/combiner network consisting of a Lange 3-dB coupler feeding a pair of Wilkinson power dividers. All thin film networks are fabricated on .015"-thick-alumina substrates. The input divider and output combiner substrates are identical in keeping with the low cost assembly philosophy. The four 4-W MMIC's are, as mentioned, fully-matched thereby eliminating post-fabrication tuning of the assembled 12-W units. The uniformity of the batch MMIC processing also eliminated the need to bin chips for matched power, gain and dc current characteristics. MMIC's were grouped, however, by lot to guarantee insertion phase uniformity and facilitate efficient power combining.

Copper-moly-copper (CMC) was selected as the carrier material of choice due to its favorable coefficient of thermal expansion, low cost and inexpensive processing (stamped versus machined). To take full cost advantage of this material, pedestals that are typically used to equalize the thickness differences between the MMIC's and thin film networks were eliminated. Instead, compensating stubs in conjunction with automated assembly techniques were employed. The capacitive stubs are used on the thin film networks and, to a lesser extent, on the 4-W MMIC's to resonate out the extra bondwire inductance resulting from production tolerances and the lack of pedestals. All of the power amplifier elements are brought together on a proprietary assembly and test fixture which accommodates the automated placement, soldering, bonding and testing of multiple units. Minimum MMIC pad sizes for automated assembly were specified before MMIC layout commenced so that they could be easily integrated into the design.

A power output distribution histogram for a "lot" of 676 12-W amplifiers is plotted in Fig. 10. As can be seen, most of the distribution is above 40.8-dBm (12-W). Typical performance of these amplifiers over the 9.3-9.41 GHz frequency

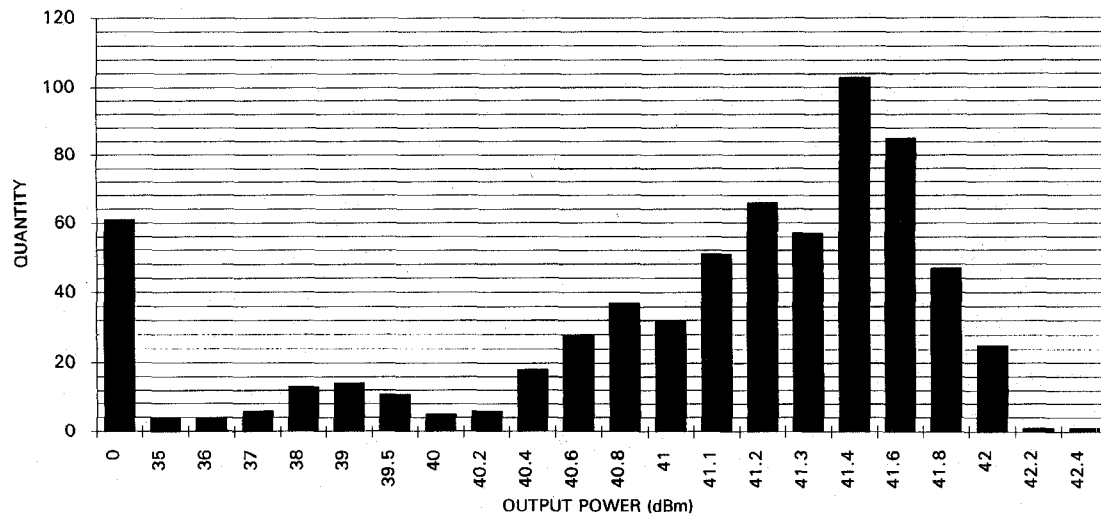


Fig. 10. Power output distribution for 676 12-W power amplifiers. The bulk of the distribution for this lot was above 40.8 dBm (12-W).

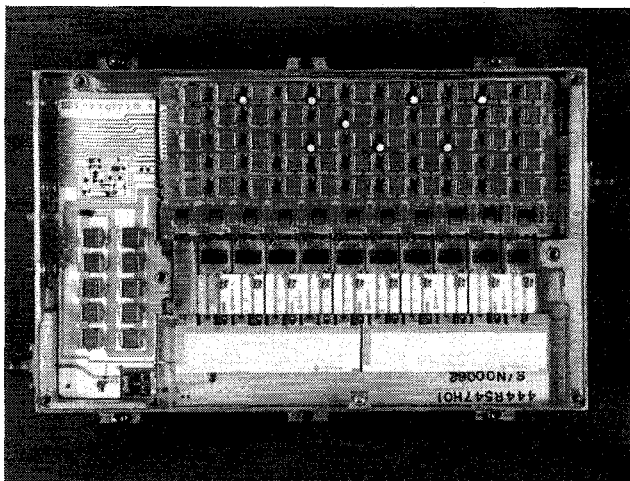


Fig. 11. Photo of an 85-W MODAR power module. Each module contains 44 of the 4-W MMIC's.

range includes 41-dBm output power with 13 dB gain and 28% power-added efficiency. Over 1700 12-W units have been delivered with a yield, defined as the percentage of the fabricated units meeting spec, of better than 85%.

#### V. 85-W POWER MODULE—160-W SOLID-STATE TRANSMITTER

A photo of an 85-W power module is shown in Fig. 11. Each 85-W module uses one of the 12-W hybrid amplifiers to drive ten additional 12-W amplifiers. The 10 amplifiers are combined using a low loss 10-way stripline serial splitter/combiner fabricated on Duroid material. Silicon pulser regulators provide both the pulsing function and the regulation of the 9-V drain voltage. Multiple 130- $\mu$ F tantalum capacitors are used for storage. The capacitors are distributed on a thickfilm substrate so that automated manufacturing techniques could be used. Fully automated production processes including epoxy dispense, pick and place and wire bonding were crucial in minimizing module fabrication time.

Excellent phase consistency of the 12-W power amplifiers along with a one-time phase set philosophy kept module "tuning" time to a minimum. The phase grouping of the amplifiers was well within a 50-degree window which allowed utilization of a passive microstrip loaded line phase trimmer to equalize the phase between amplifier channels. Phase compensation from 10–60 degrees in 5-degree increments is achievable by removing appropriate wire bonds in the module. At the present time, approximately 80% of the power modules do not require the phase compensation.

The MODAR transmitter delivers 160-W of peak output power by combining two of the 85-W power modules which are driven by an external amplifier. The three separate gain blocks distribute the gain and minimize feedback which could lead to oscillations. The two power modules are combined using a branchline power combiner. The transmitter was designed to accommodate multiple pulse modes (pulsewidths between .01–260- $\mu$ sec with duty cycles from 1–8%). Typical gain over the 9.3 to 9.41-GHz frequency range is 50 dB, 28 dB from the driver amplifier and 23 dB from the power modules.

Reliability of the solid-state transmitter was evaluated by performing an on-off cycle life test of an 85-W module. The unit was powered on for 5 minutes and then turned off for 5 minutes. While on, the unit was pulsed (5.2- $\mu$ sec, 8% duty cycle) with RF at an input power of 28 dBm. After 171 days and approximately 25 000 cycles, the unit still met all specifications for system insertion. The module was also *g*-tested at 2000 g's without failure. Of the 75 solid-state transmitters delivered to date none have been returned for MMIC related failures.

#### VI. CONCLUSION

A high yield 4-W X-band power MMIC has been designed and produced for insertion into the MODAR weather system. To date, over 15 000 MMIC's have been delivered with a combined dc/RF yield averaging 39%. System architecture design and concurrent engineering efforts involving the higher level 12-W amplifier and 85-W power module assemblies were

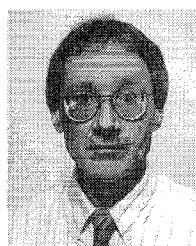
crucial in achieving high MMIC yields without sacrificing system performance. This work clearly demonstrates the viability from a cost, performance and reliability standpoint of power MMIC insertion into commercial systems.

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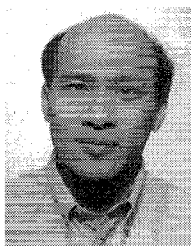
In 1977, he joined the Microwave Circuit Development Group at Westinghouse Electric Corp., Baltimore, MD, where he worked on various hybrid and monolithic MIC designs and component model-

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During 1972–74, he was employed as an engineer by Cincinnati Electronics Corporation, Cincinnati, Ohio, and engaged in fabrication of CdS infrared detectors. From 1974 to 1976 he was a project engineer for Turnbull Control Systems division of Eurotherm, Ltd., Worthing, Sussex, UK, involved in electronic control system design, test, and installation. Following completion of his education, from 1979 to 1982, he was employed by Texas Instruments, Dallas, Texas, his last assignment being as Member Technical Staff working on development of direct-write processing for silicon memories. Since 1982, He has been with the Westinghouse Advanced Technology Laboratories in Linthicum, MD, working in GaAs MMIC development. Among other assignments, he has been involved in GaAs power MESFET work from the development stage to MMIC manufacturing. Current interests include PHEMT development and manufacturing technology.



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**Mark Pingor**, photograph and biography not available at the time of publication.



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